

IN THE DRAWINGS

Proposed changes to Figs. 2, 3, 5, 6, 8, 11, 14, 15, 17, 18, 20, 23, 26, 27, 31, 34, 35, 40, 41, 44, and 45 are submitted herewith, with a Letter to the Official Draftsman.

REMARKS

Reconsideration and allowance of this application are respectfully requested in light of the above amendments and the following remarks.

Proposed changes to Figs. 2, 3, 5, 6, 8, 11, 14, 15, 17, 18, 20, 23, 26, 27, 31, 34, 35, 40, 41, 44, and 45 are submitted herewith, along with Replacement Sheets, to overcome the objections thereto. The figures have been amended to contain directional flow arrows.

Claim 1 has been amended to highlight patentable aspects of the invention. Non-elected claims 3-17 have been canceled. Support for the subject matter of amended claim 1 is provided at least in paragraph [0092] of the specification on page 22, lines 8-15.

Claims 1 and 2 were rejected, under 35 USC §102(e) as being anticipated by Tanaka (US 6,505,334).

To the extent that these rejections may be deemed applicable to the amended claims, the Applicants respectfully traverse, based on the following points.

Claim 1 now recites checking the ratio between the layout of wires in a chip layout and the layout of contact holes in the wires so as to detect wire formation defects in a semiconductor device.

In an exemplary but non-limiting embodiment of the invention, the ratio may be defined by the area of the contact holes in the wires to the area of the layout of the wires. In another exemplary but non-limiting embodiment, the ratio may be defined by the number of contact holes in the wires to the number of wires.

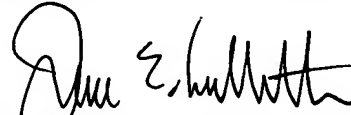
By contrast to the claimed subject matter, Tanaka discloses monitoring the wiring density of an integrated circuit layer and employing contact holes to route layout wiring to a different layer of the integrated circuit so as to prevent the wiring density of the monitored layer from exceeding an upper limit value (see Tanaka abstract and col. 2, lines 31-36). Tanaka does not disclose the claimed feature of checking the ratio between the layout of wires in a chip layout and the layout of contact holes in the wires so as to detect wire formation defects in a semiconductor device.

Accordingly, the Applicants submit that Tanaka does not anticipate the subject matter defined by claim 1. Therefore, allowance of claim 1 and dependent claim 2 is warranted.

In view of the above, it is submitted that this application is in condition for allowance and a notice to that effect is respectfully solicited.

If any issues remain which may best be resolved through a telephone communication, the Examiner is requested to telephone the undersigned at the local Washington, D.C. telephone number listed below.

Respectfully submitted,



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Date: March 6, 2006
JEL/DWW/att

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FIG. 2

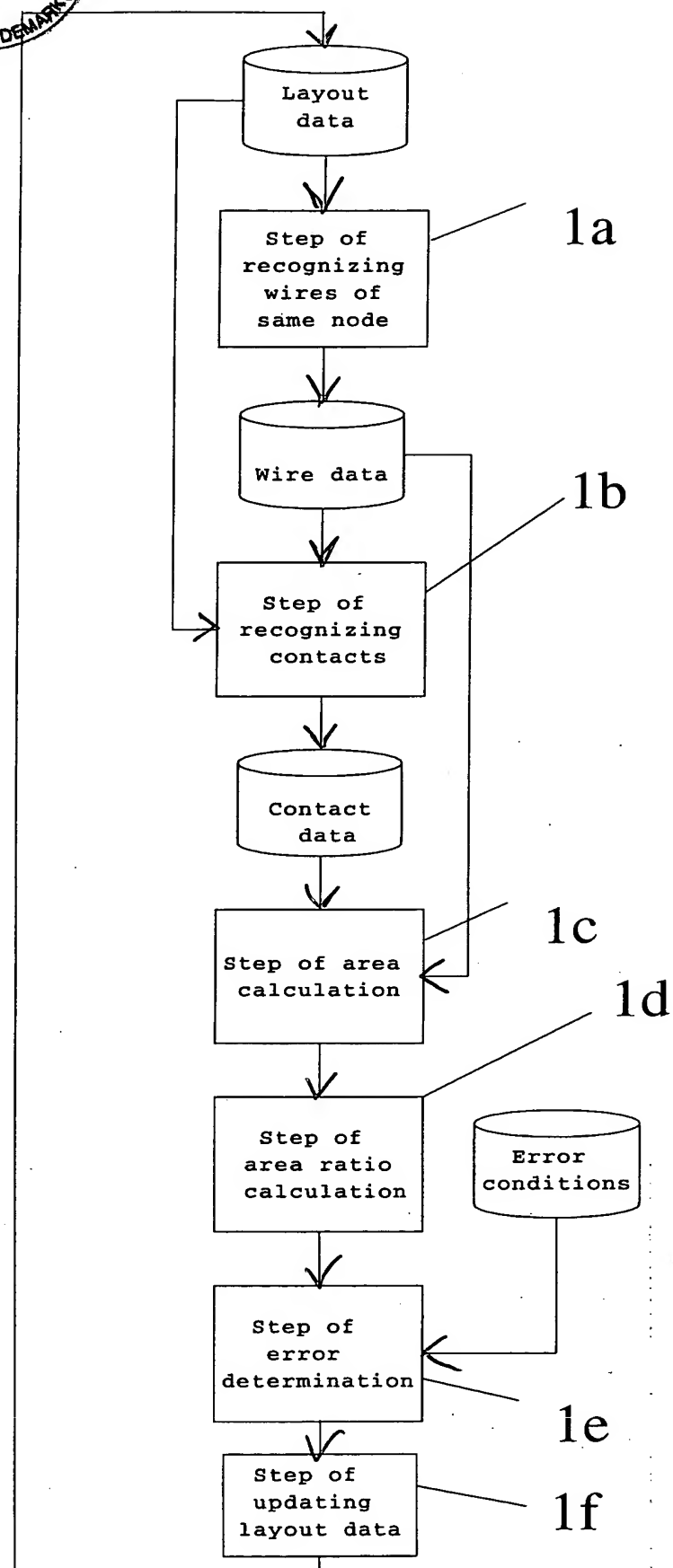


FIG. 3

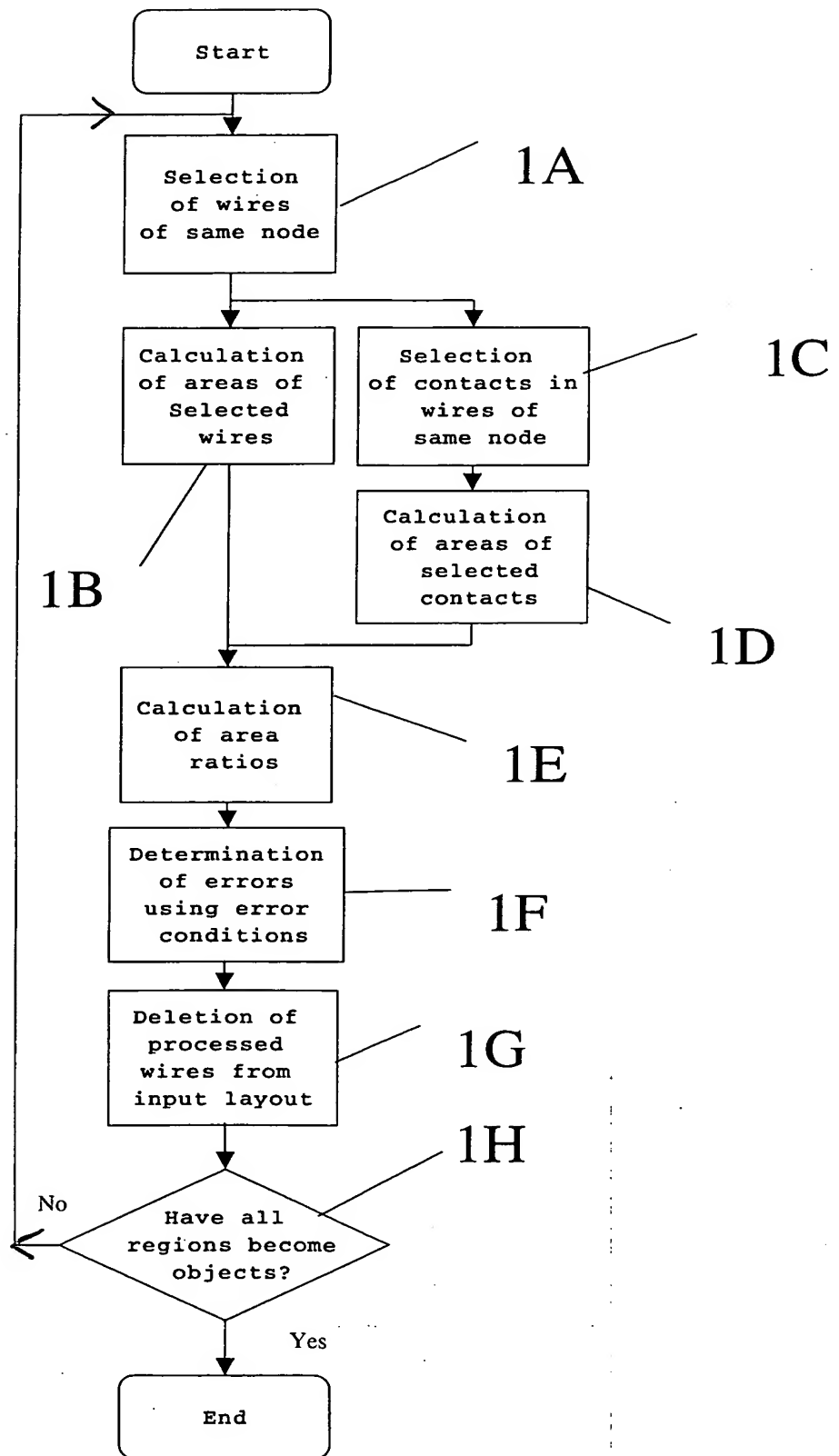


FIG. 5

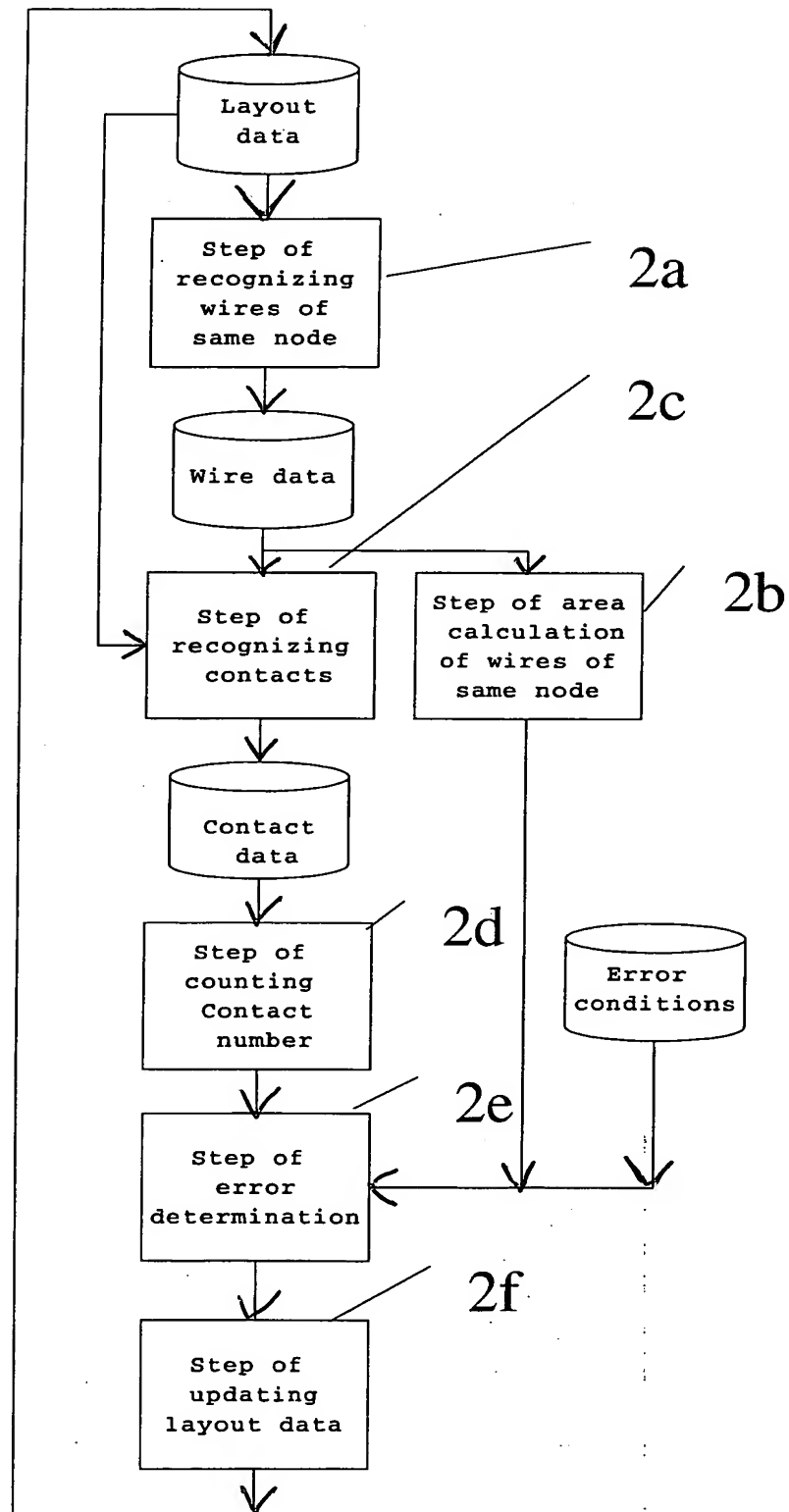


FIG. 6

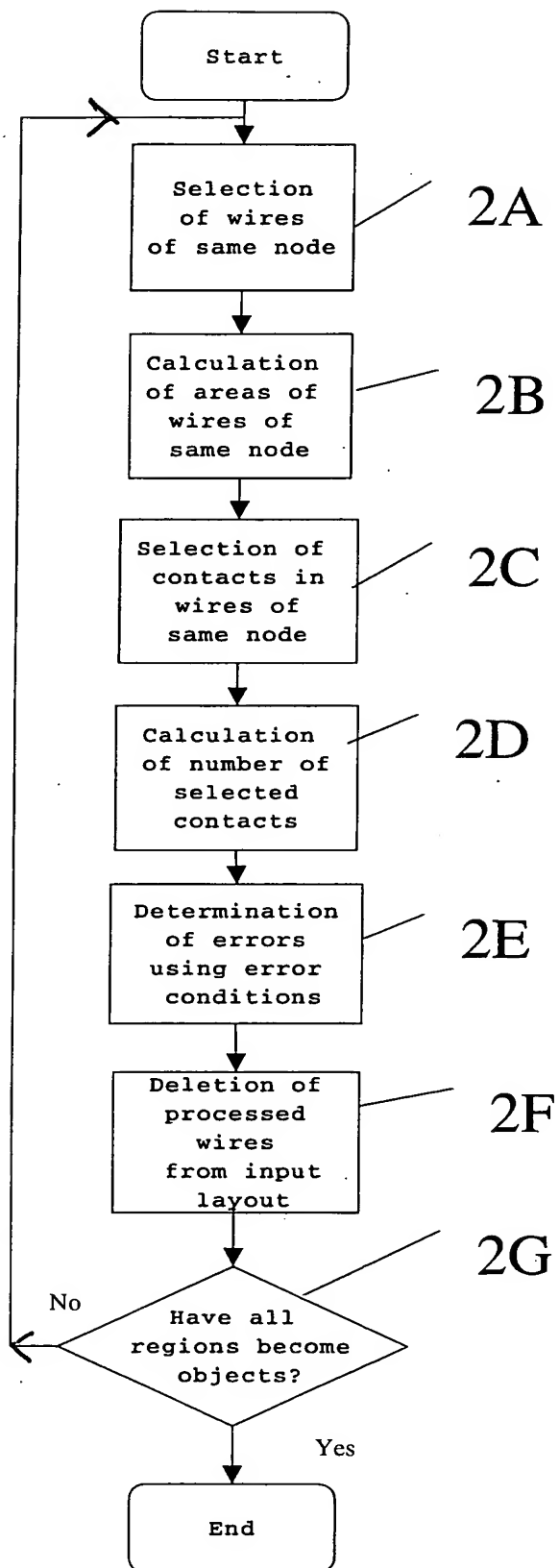


FIG. 8

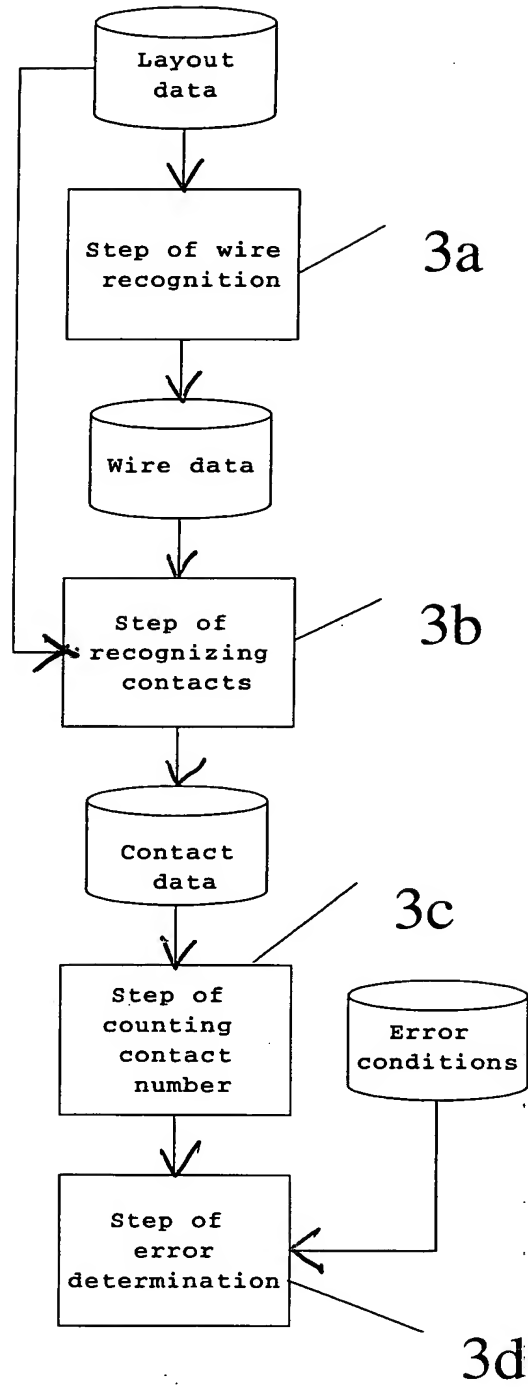


FIG. 11

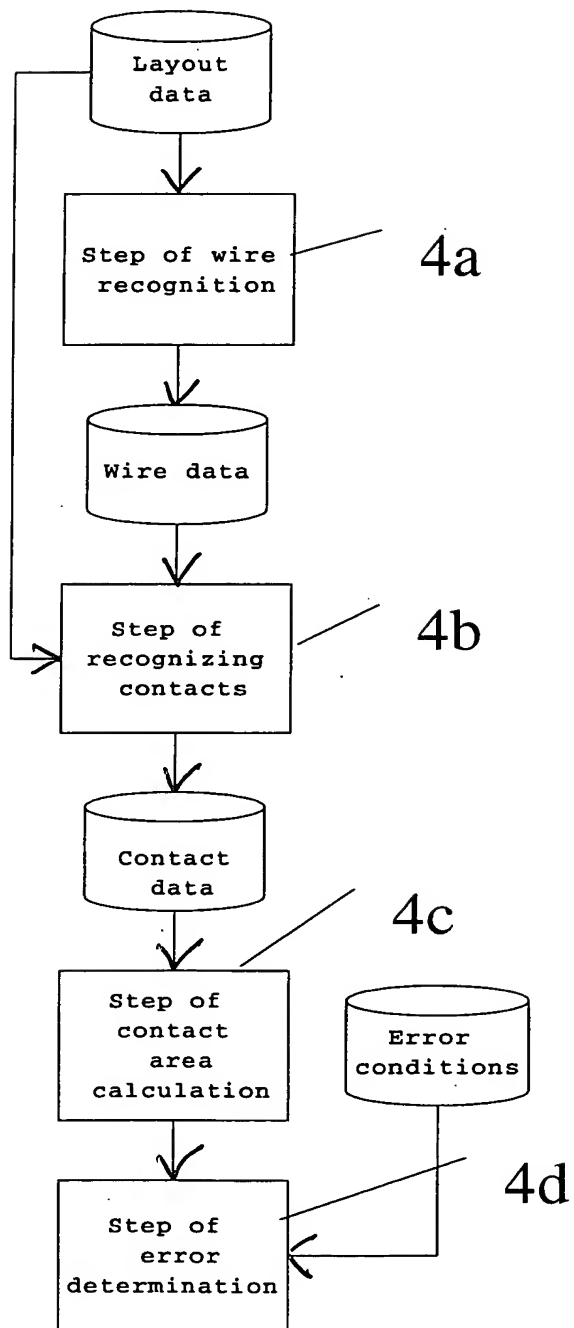


FIG. 14

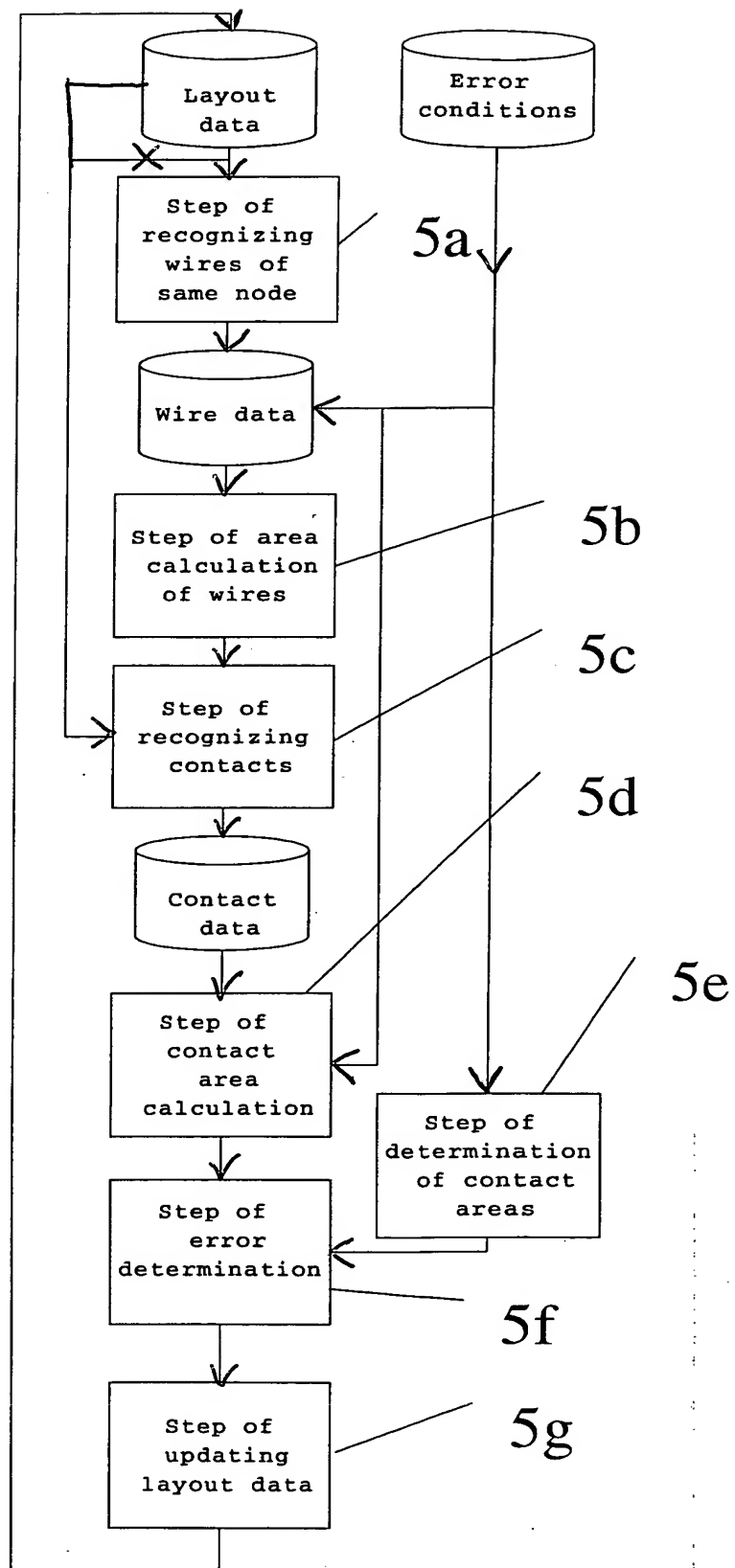


FIG. 15

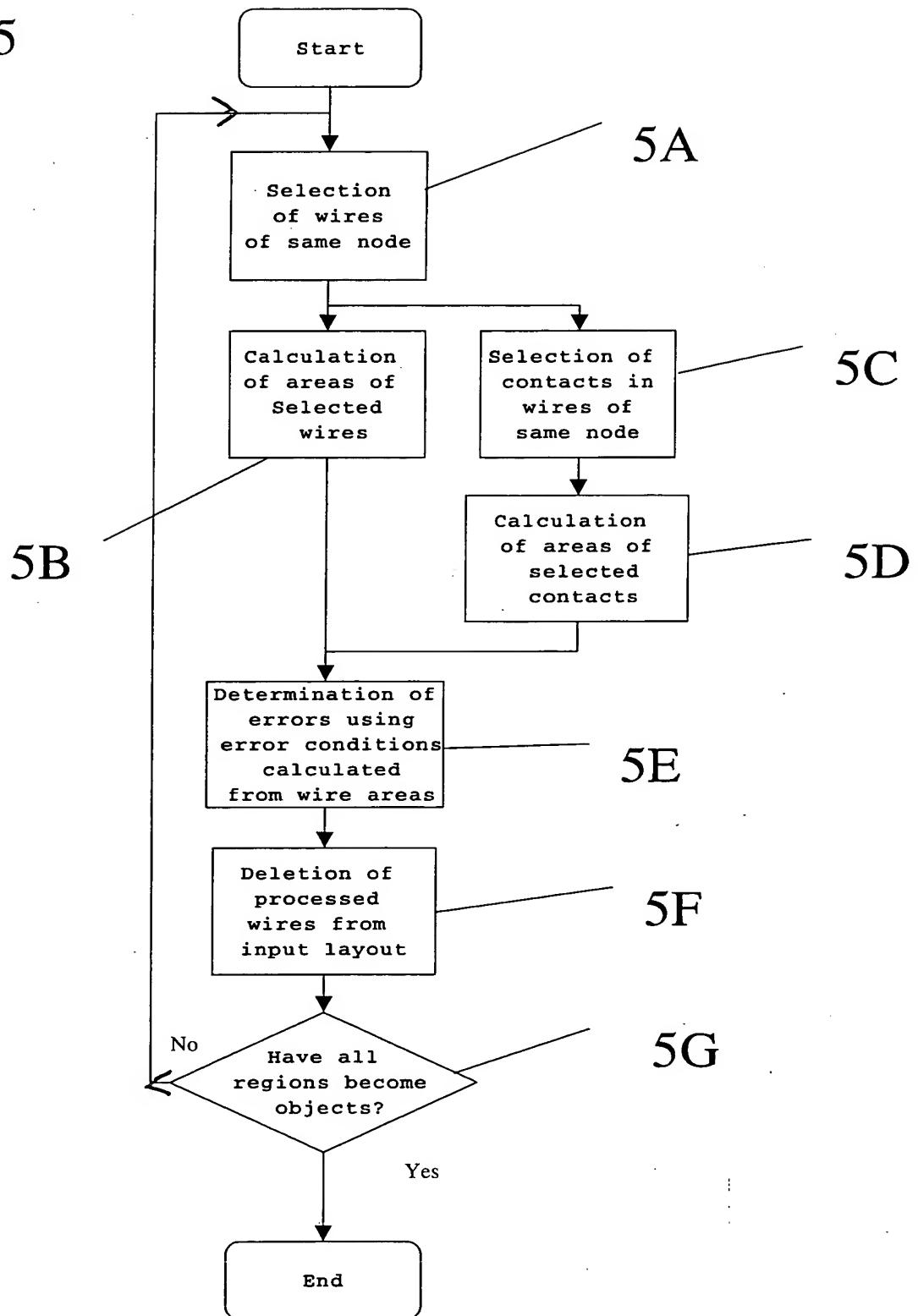


FIG. 17

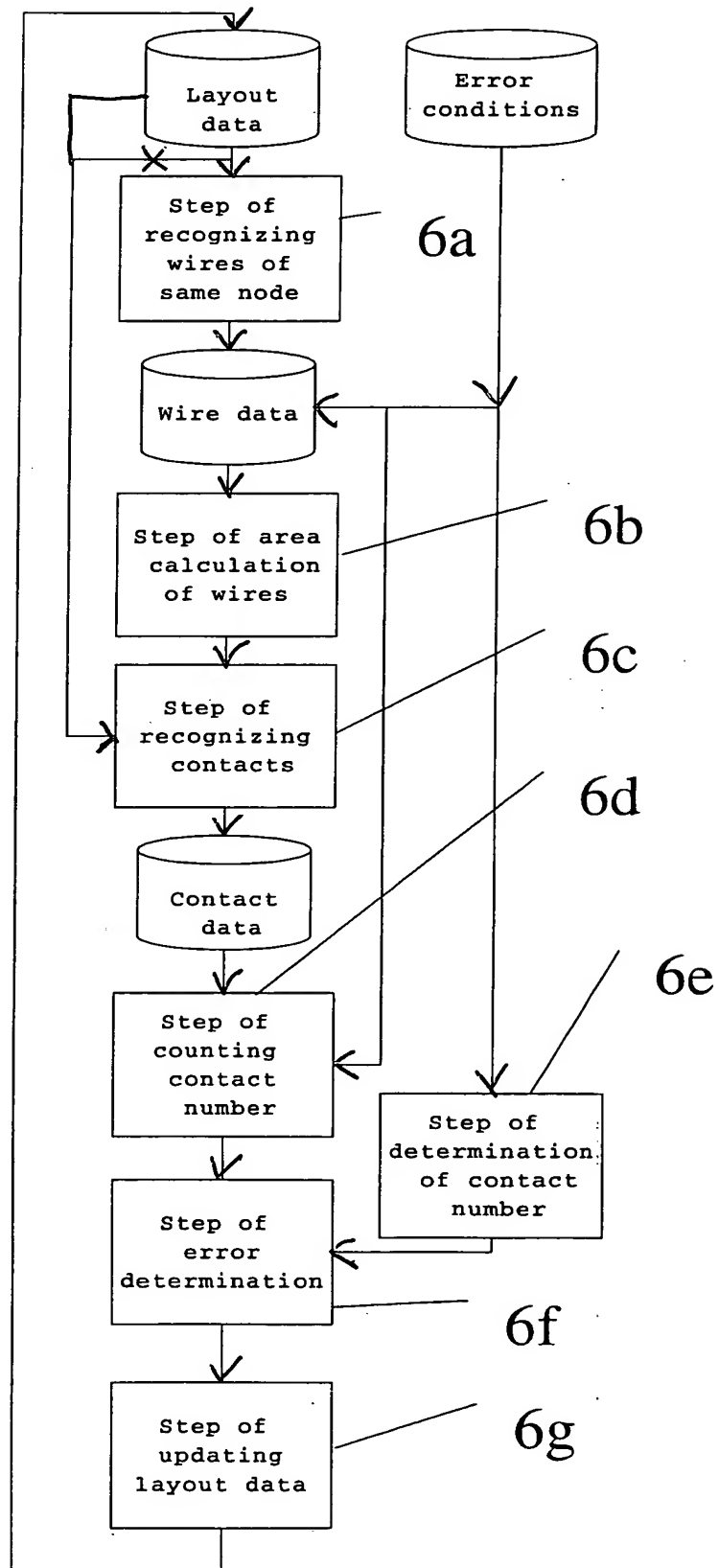


FIG. 18

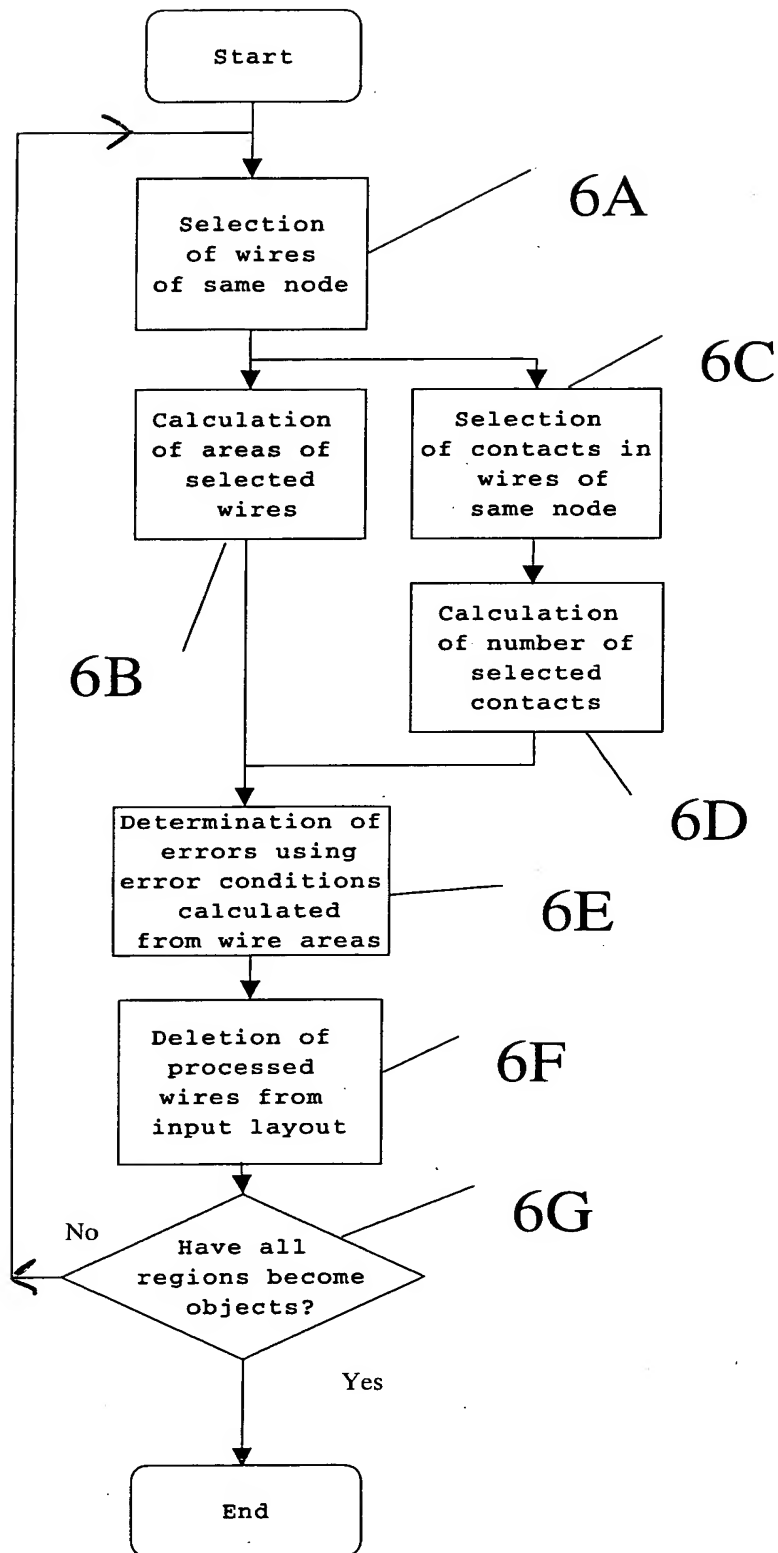


FIG. 20

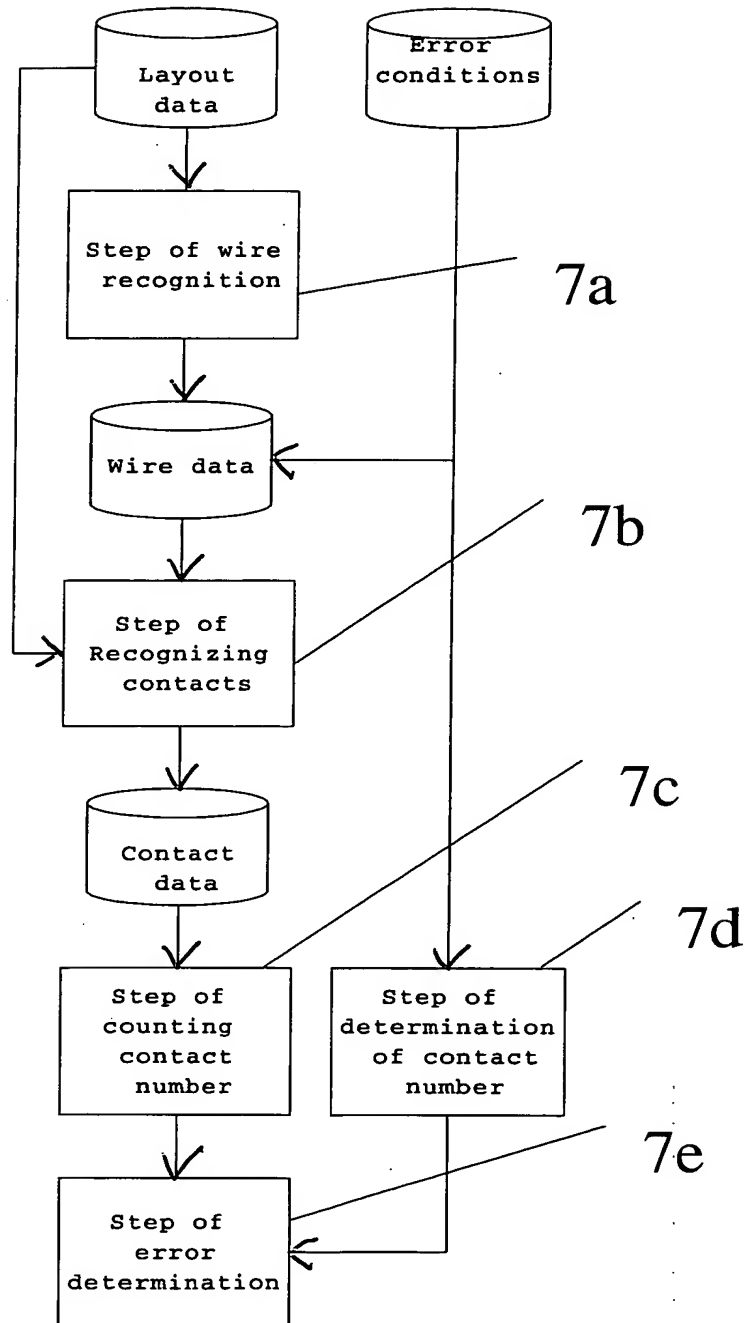


FIG. 23

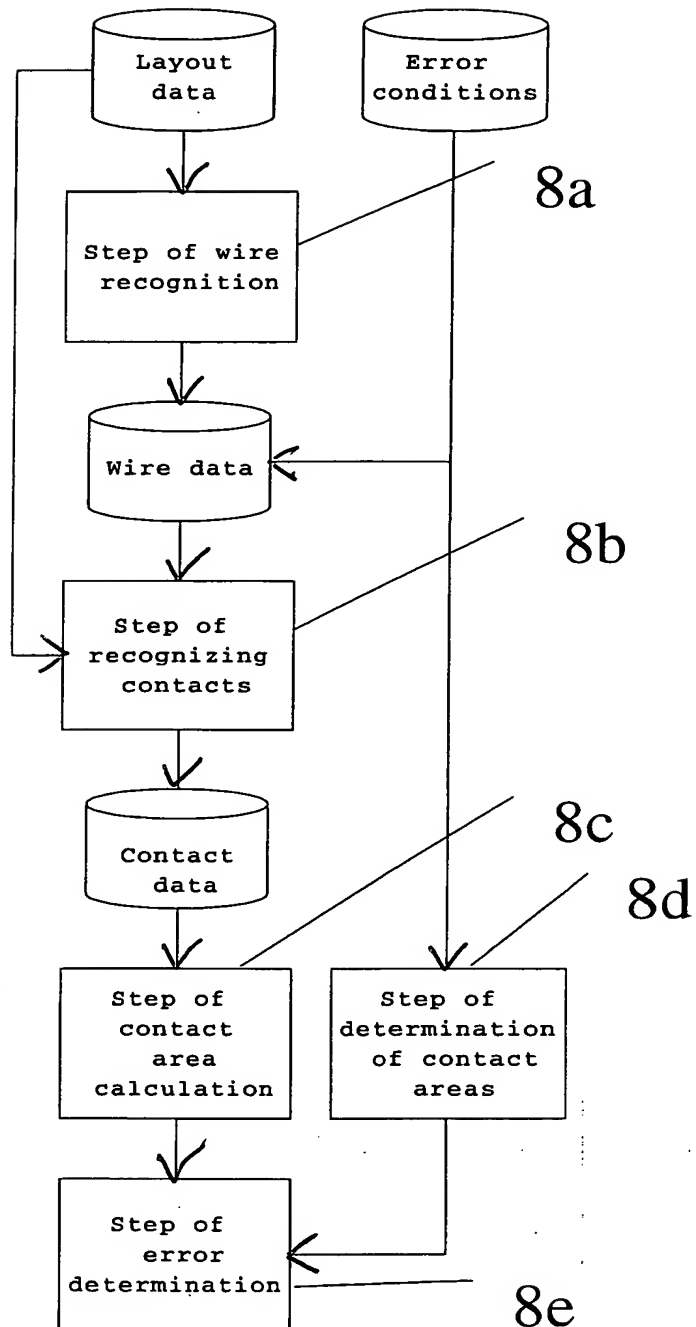


FIG. 26

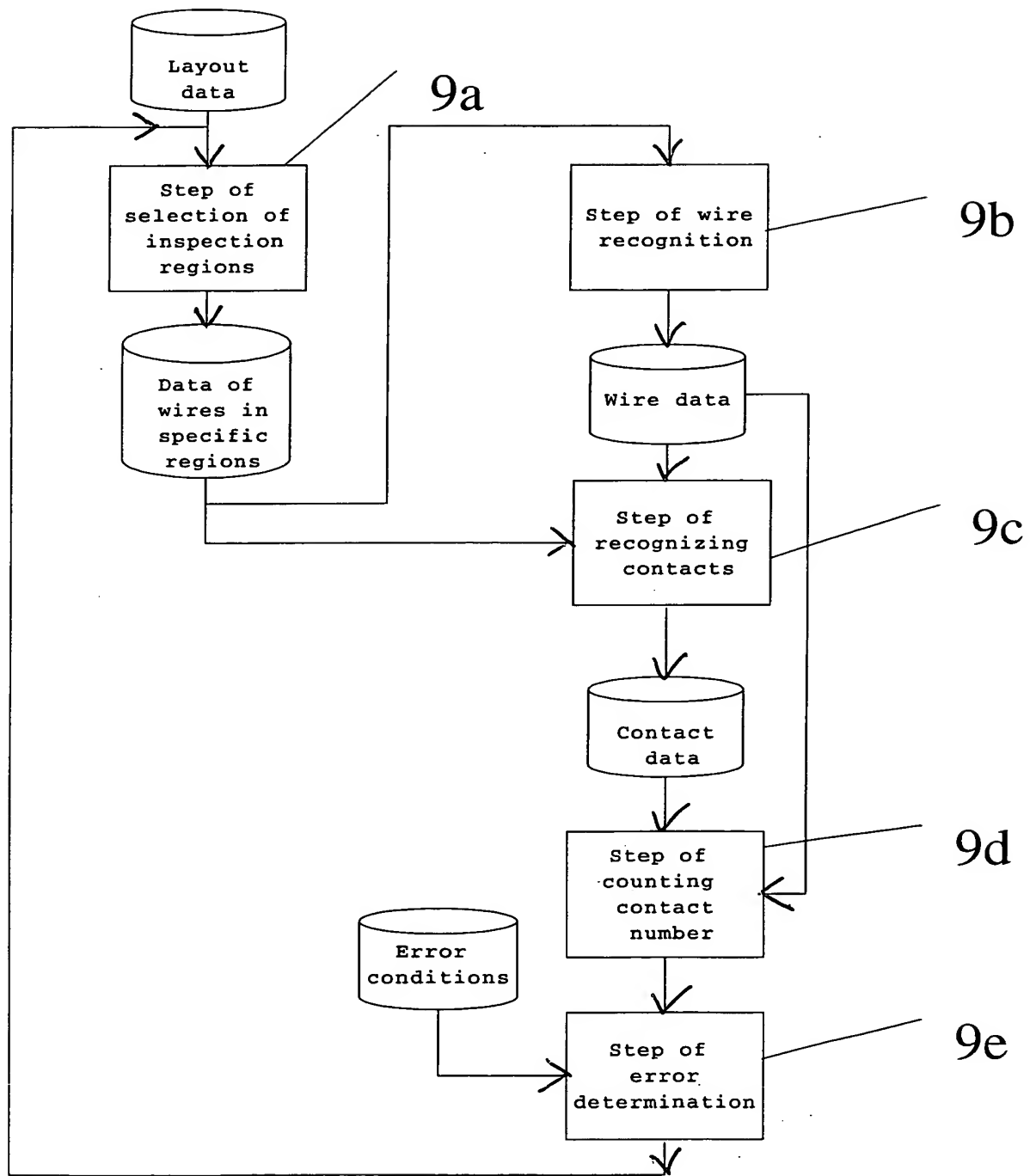


FIG. 27

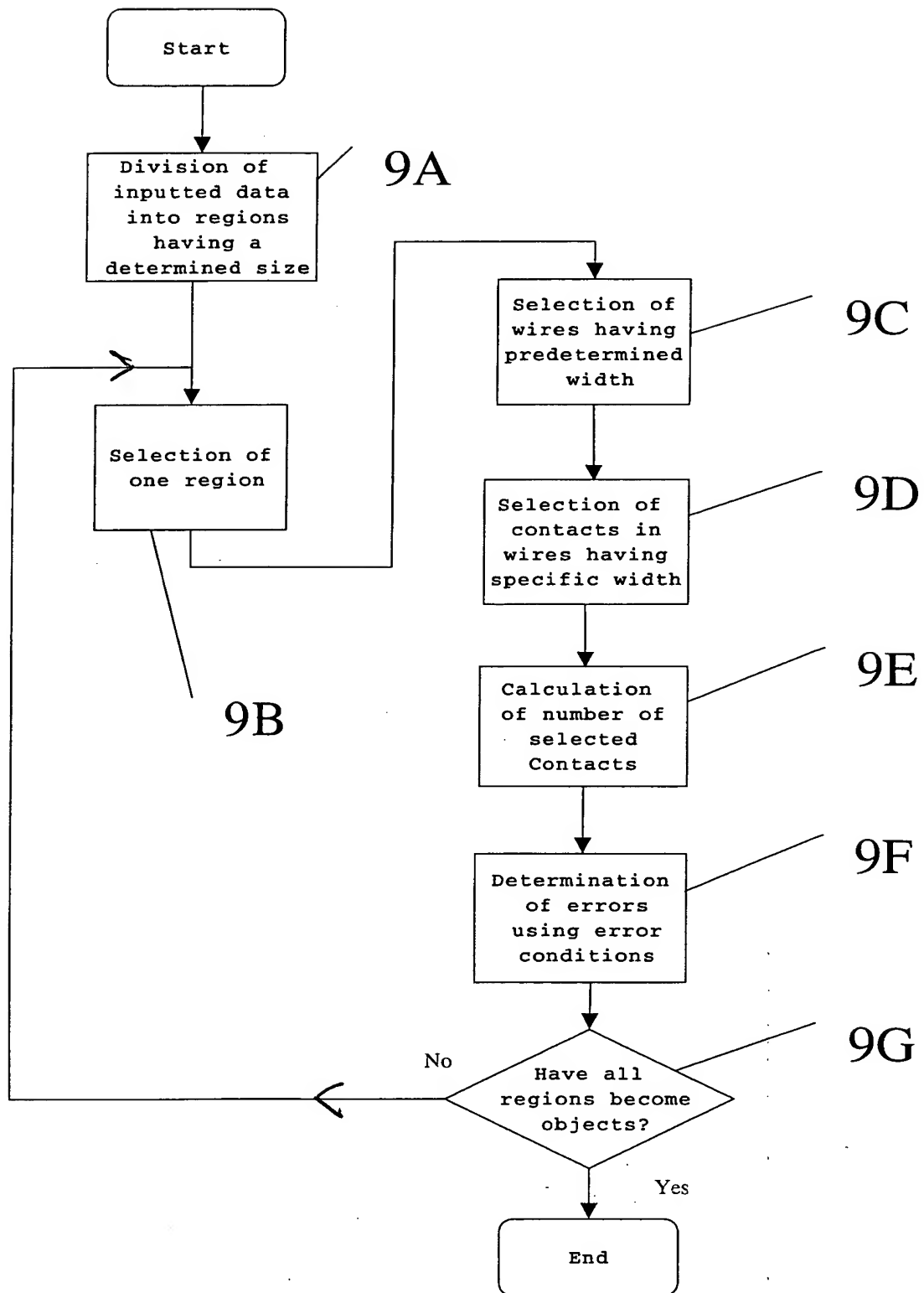


FIG. 31

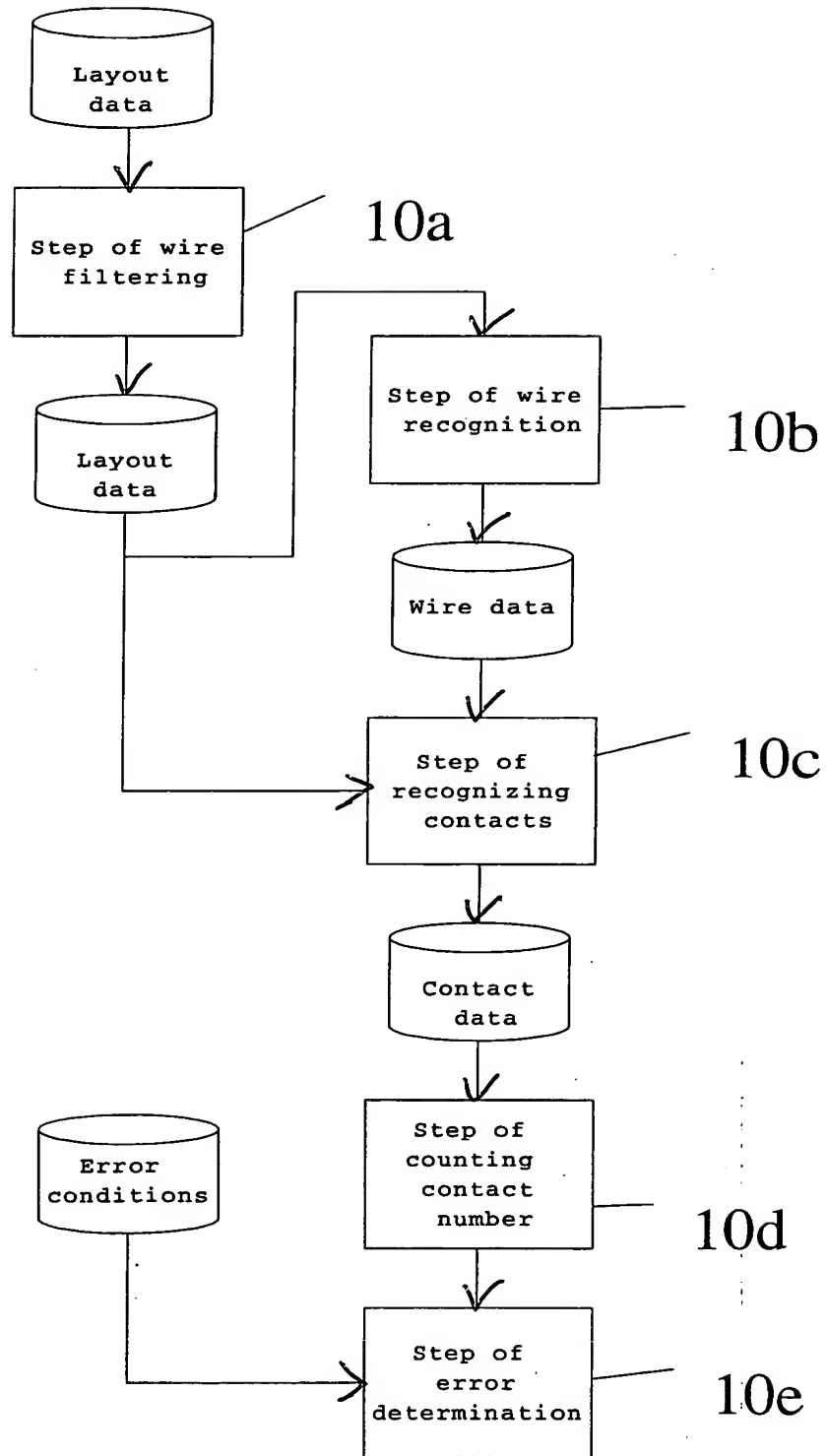


FIG. 34

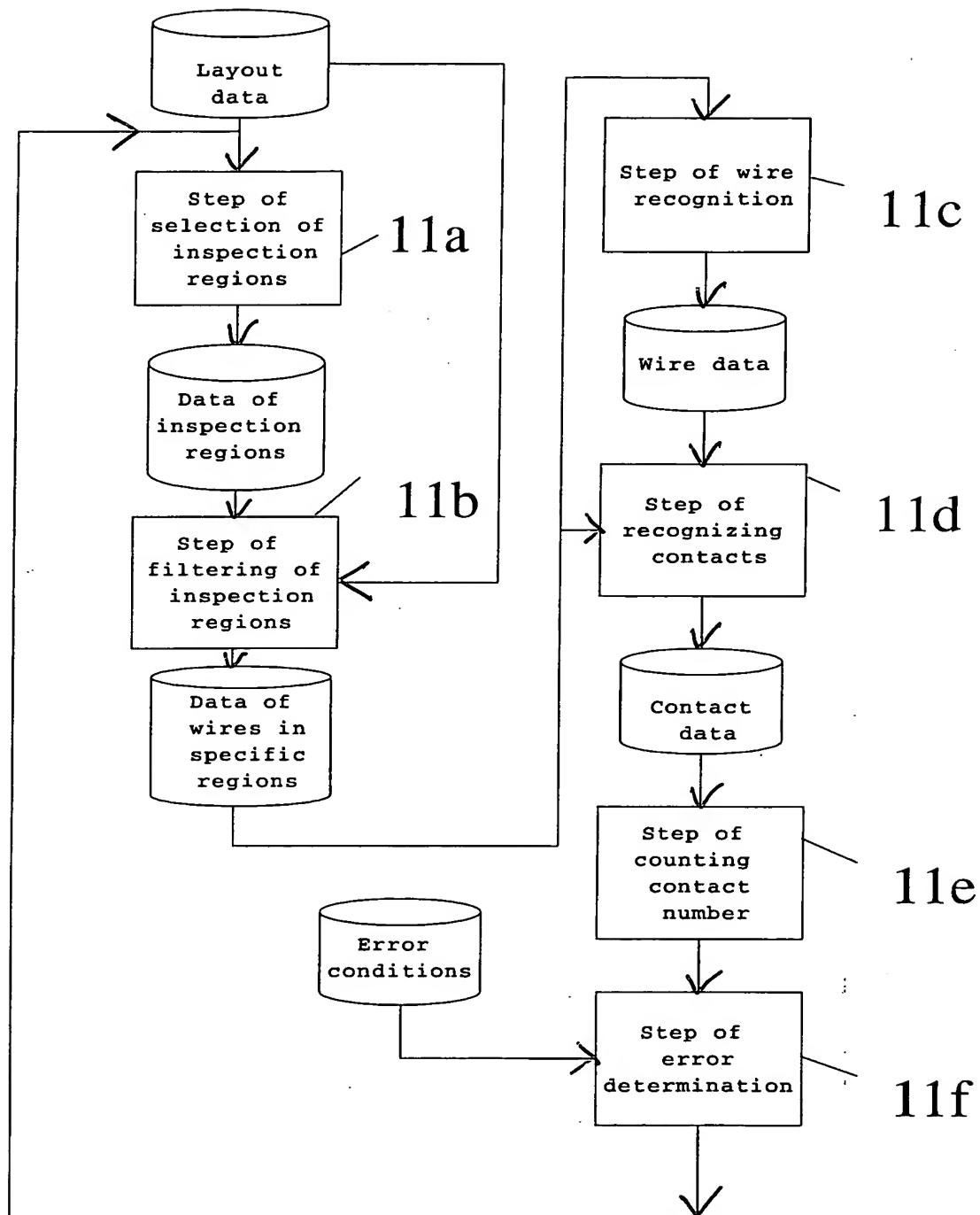


FIG. 35

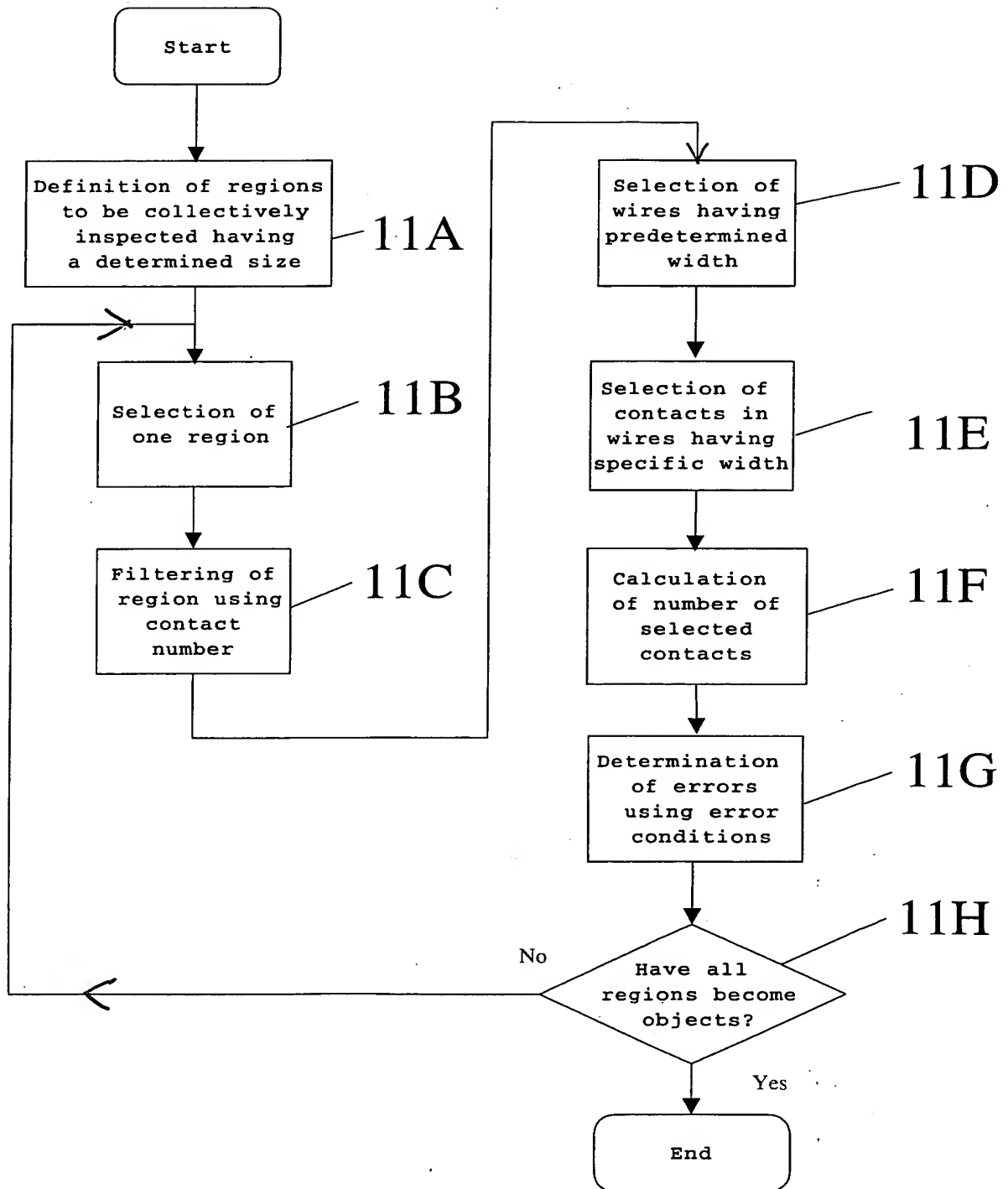


FIG. 40

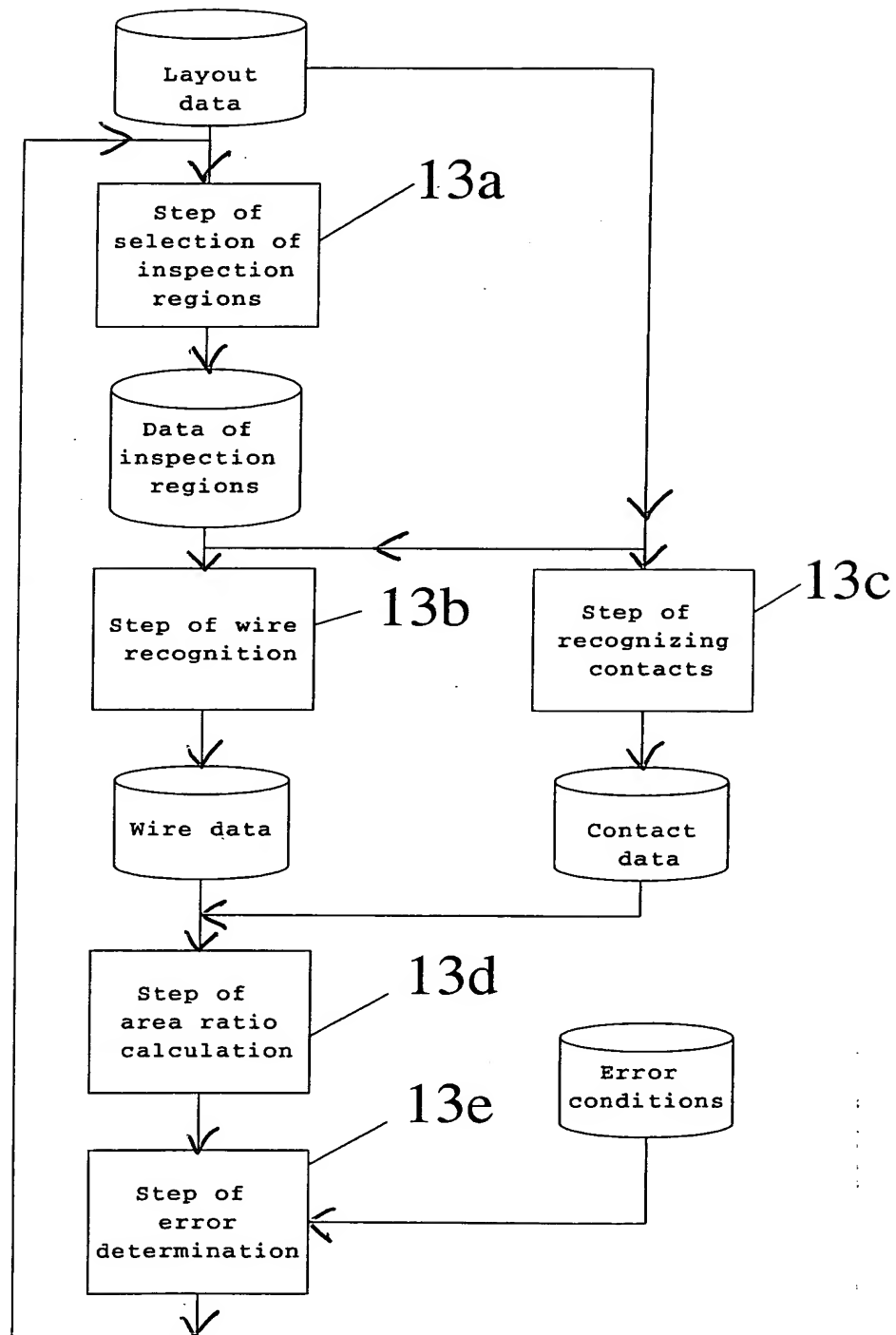


FIG. 41

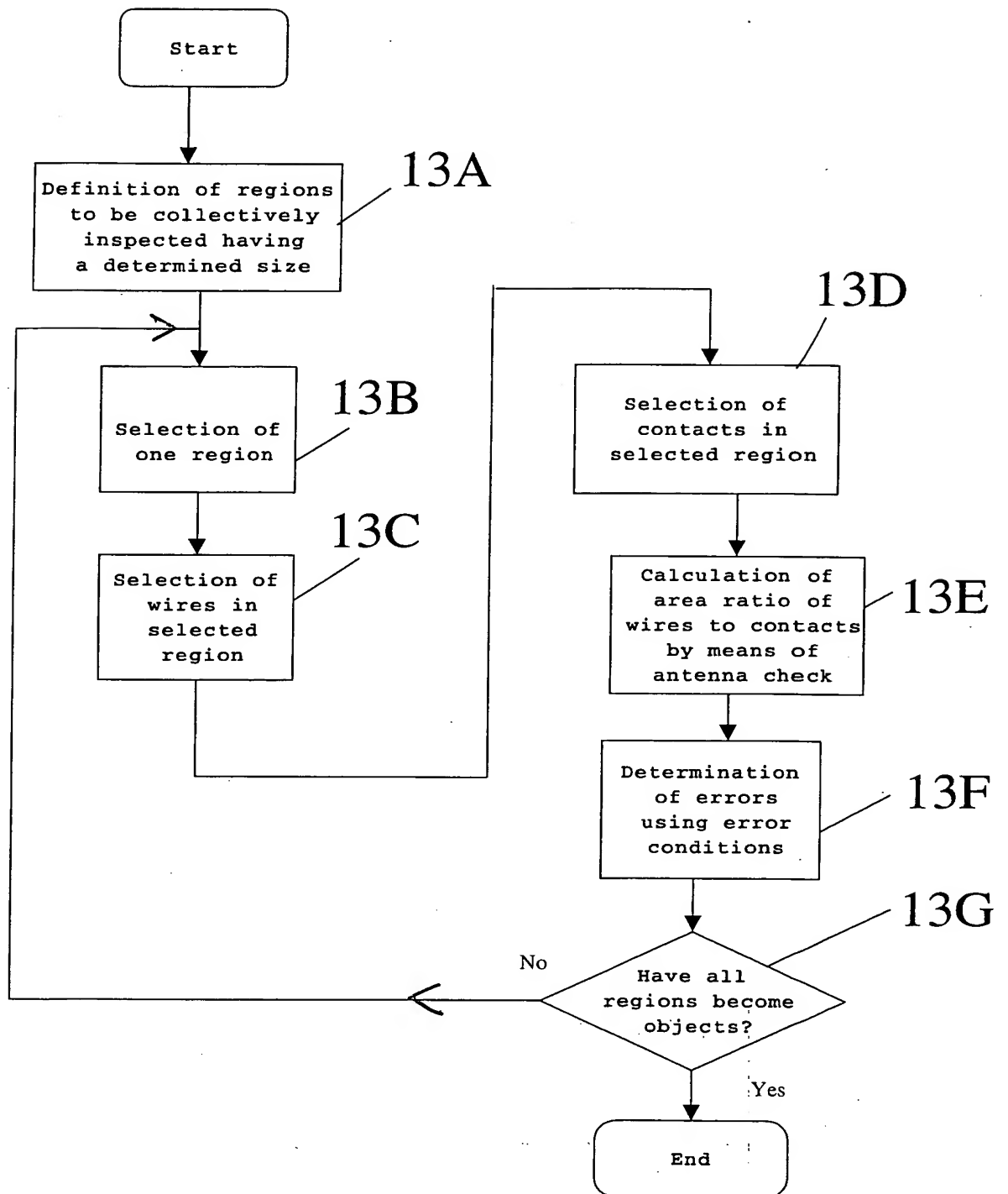


FIG. 44

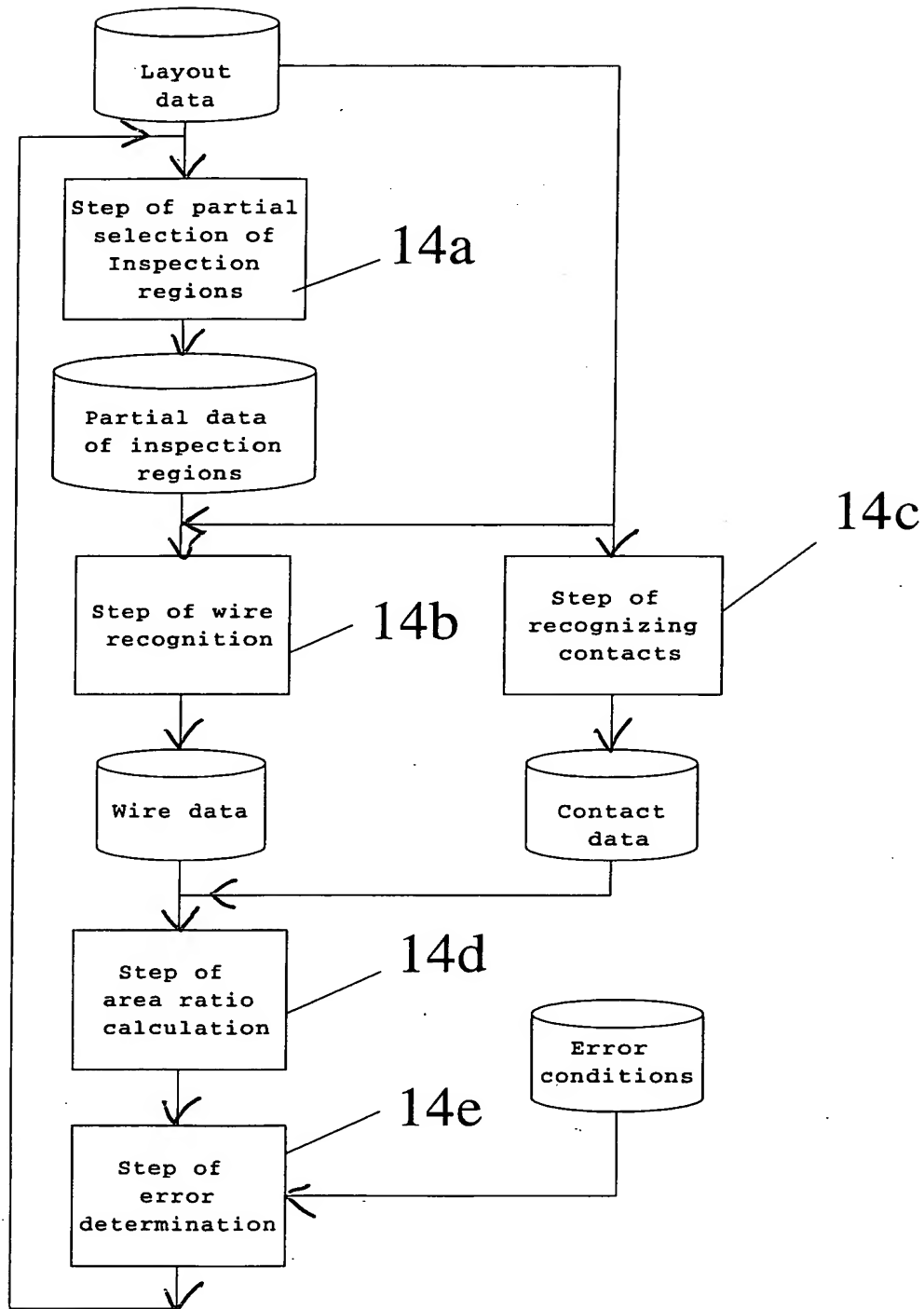


FIG. 45

